Optoelectronic Materials and Devices
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Lecture - 36
MOS Capacitor

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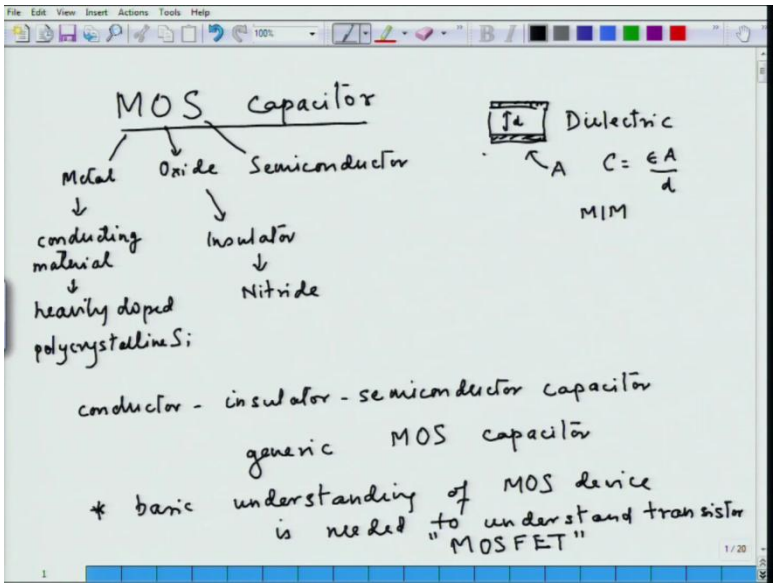

Today we will discuss a very important device MOS Capacitor. MOS capacitor stands for Metal Oxide Semiconductor. In module 2, you would have learnt about capacitors, which are made of only dielectric material, there are the capacitor was a dielectric material which was contacted by two metals on the two side, these were the metals. And you learnt that the capacitance here is given by epsilon A is the area here, is A is the area of the capacitor divided by d, and d is the thickness.

Today, we will discuss a device which is not simply; this is normally referred as Metal Insulator Metal - MIM device. Today, we will discuss a device which is MOS where the M stands for Metal, and O stands for Oxide, and S stands for the Semiconductor. Now, although, this is we continue to use a term MOS capacitor in the literature very often metal is replaced by some other conducting layer, conducting material, for example heavily doped p-type polycrystalline silicon.

And very often oxide is not an oxide, it may be another insulator for example, a nitride, a silicon nitride layer or some other insulator. In that case we should probably use the term

here, which would be conductor, insulator, semiconductor capacitor, but that would be very lengthy. And hence although, we may change the identity of M and O we continue to use the acronym MOS capacitor and just keep in mind that, that does not mean that metal has to be normally a metal. So, we will continue to use the generic name, for this kind of devices as MOS capacitor.

Now, if we start discussion on this particular aspect, we will have to first see why we need to learn it. So, we in the beginning we said there are 3 of 4 important devices in integrated circuits, resistors, diodes, capacitors and transistor. So, this is another kind of a capacitor that we make in integrated circuits. So, it has it is own application, as a capacitor we will see later in this lecture, that it has many applications, but in addition to that, this is understanding of the MOS capacitor is basically required, the basic understanding is required, to understand of MOS device is needed to understand transistors.

Because, today in integrated circuits one of the most common transistor that is used is MOSFET and as you can see in the name it is Metal Oxide Semiconductor Field Effect Transistor. So, we can start discussion only on transistor only, if we understand the MOS fundamental. So, the importance of MOS capacitor is not only as a device in itself, but also as, it is a very important component of the MOSFET devices also.

So, in today's lecture, we are going to cover these aspects, we will look at the ideal MOS capacitor how does it give the capacitance, we will look at how we estimate the threshold voltage, which is a important parameter for these MOS devices. Then we will look at what are some of the non ideal ties we really do not have time to get into the details of that, but we will see the effect of some of the non ideal ties here and then we will see some of the applications of the MOS capacitor, in the electronic devices.

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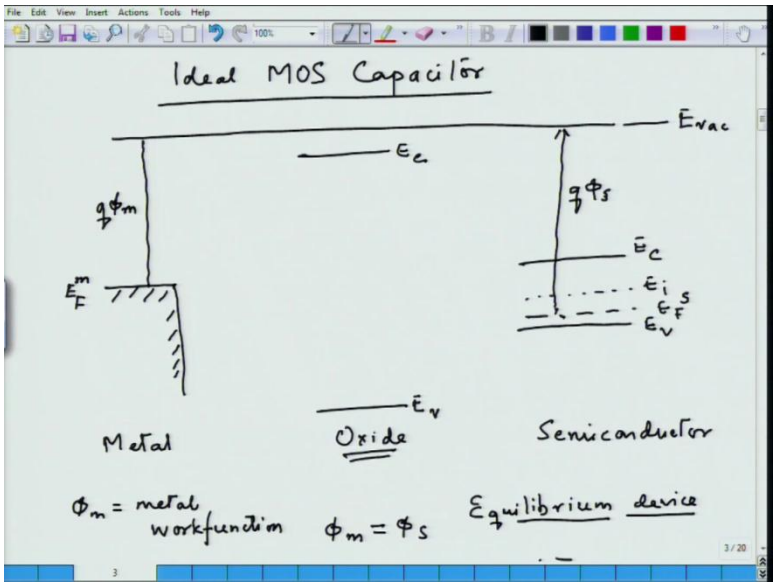

So, let us start with the ideal MOS capacitor, the ideal MOS capacitor is defined in terms of certain parameters. So, we have a metal in the ideal MOS capacitor, we have the oxide and we have the semiconductor and let me, first draw individually what they are electronic structures are in order to define the electronic structure. If you will recall in the beginning we said that all the energies, are referred with respect to a vacuum level, with respect to this vacuum level for metals, we have Fermi energy, we have continuous bands and Fermi energy defines for the metal the electronic structure.

In this definition for Fermi energy is the energy required to take the electron from the metal to make it free is the is the work function metal work function. So, phi m is the metal work function and this is all with reference to the vacuum level, if you look at the oxide, oxide is basically a very wide band gap, you can think of it as a very wide band gap semiconductor. And if I we look at the semiconductor, it is a intermediate band gap material which has conduction band valence band.

We define a intrinsic level, in the centre and we define a Fermi level and let me take the example of a p-type semiconductor here, Fermi level inside the semiconductor. And then we define the work function for semiconductor, as the energy required to take a electron from the Fermi level of the semiconductor to the vacuum level is given by q of phi s.

So, now if we try to bring these three components together, metal oxide and semiconductor, we need to see how they will align with each other, this is something

similar to what we did in the diode. So, if you first look at the equilibrium structure and then when then we see if we apply a bias to that device what will happen and what kind of activities will happen inside the device.

Interestingly in the p-n junction, when you apply a bias a current is flowing and hence we have to have a dynamic type of estimation in order to figure out what is happening inside the device, which makes it difficult. But, capacitor is a equilibrium device, it is a equilibrium device, because capacitor unless we are changing voltage from one voltage to the other, voltage in in transient state there is no current flowing.

The the oxide part is basically a insulator, which does not allows since there is a huge gap for electrons to go through the insulator to the metal or through the for holes to move through the valence band of the oxide. It basically there is no current flowing in a capacitor when a certain bias or no bias is applied, it is only when we change the bias may be there is a current transient, current that flows which. And in this course you will not consider because you can pretty much do a whole course, on MOS devices independently.

So, capacitors are in that sense a little bit easier, since the equilibrium statistics can give us most of the information that we need for the purpose of this lecture. So, this is basically equilibrium device in that sense, for a given bias we can get information about the capacitor. So, when I try to bring this together, we know in equilibrium what happens is that Fermi level should align.

Now, in order to make a ideal moss capacitor I am going to put the requirement that, the work function for the metal is equal to work function of semiconductor. So, the Fermi levels of the metals and the semiconductor are already aligned.

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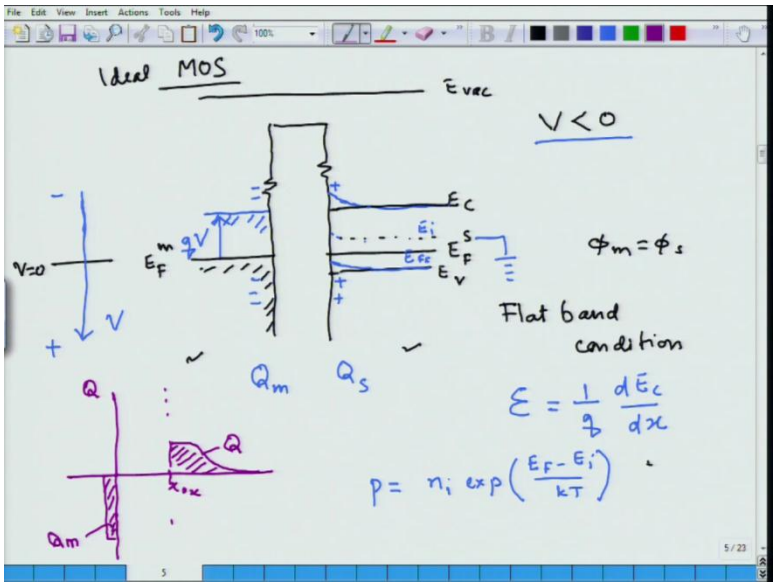

So, if I do that then I can I will plot the combined electronic structure of a MOS capacitor, as the metal, the insulator in between the Fermi level of the semiconductor. And since, phi m is equal to phi s the they they are they are normally aligned with respect to the vacuum level and from now onwards I will not plot it the vacuum level all the time you just, you remember that this is all the numbers are relative to the vacuum level.

So, for ideal MOS capacitor phi m is equal to phi s and this means that my valence band starts here, my intrinsic Fermi level is here and this is my conduction band and in between I have the semiconductor sorry oxide. Now, in this situations since, we have this ideal MOS condition, there is no charge accumulation in either in the metal side and this is known as the flat band condition.

The bands remain flat there is no bending of the bands, as we bring the metal oxide and semiconductor together and at this point there is, this is in equilibrium and no voltage is applied V is zero. So, if V is 0 this would be my electronic structure in equilibrium for metal oxide, ideal metal oxide semiconductor. Now, I would like to see the situation if I apply a bias to it because as I said in each case I can look at the equilibrium situation and see what happens.

So, if I apply a bias. So, if I am going to apply a bias, let us look at the condition of applying a bias, in which I am going to start with voltage I am going to start with the

voltage which is going to be negative, voltage is less than 0, if I do that then what is going to happen here, basically what I am saying is I will apply a voltage less than 0 with respect to a p-type semiconductor.

So, if I am taking this at ground, the semiconductor at the ground I am saying that the voltage applied, in the flat band condition the voltage there is no voltage applied v is equal to 0 and in the now, I am looking at a situation when I will apply a voltage with respect to this ground. So, if I apply a negative voltage, then it is in this direction the and if I apply positive voltage, it is increasing in this direction. So, the voltage is applied in this direction.

So, let us look at the first situation, when V is less than 0 which means the applied voltage is, in this direction, when I apply a electrostatic potential which is negative with respect to the semiconductor, which basically means that for the holes the electrostatic potential is negative on the metal side. So, if I am looking at the the energy band diagram, for the electron it is it says that I am going to move this Fermi level, up by I am going to move this Fermi level up by the amount q and the applied voltage.

When I am moving the Fermi level up what will happen I am biasing this negative with respect to the p type semiconductor, which basically means that my holes are going to be attracted towards a metal electrode and I am going to have a positive charge. So, if I am moving this up, my Fermi level is going to remain same because once I have applied the voltage again it is a equilibrium situation, there is no current flowing.

So, the Fermi level of the semiconductor would remain same, but the other the other energy structure for valence and conduction band is going to going to increase and band forward on top of this, if I have this situation basically it says that I have more holes here. Because, now what I have done is my Fermi level which is constant, is going to be moving closer to the intrinsic level and I am going to have positive charge accumulation over the semiconductor side and equivalent to this positive charge accumulation, I will have a negative charge on the metal side.

Now, because of this positive charge I am going to call this as, the charge on the metal side and this the charge on the semiconductor side and this charge is going to lead to a capacitance, across this oxide. Now, since I have applied a voltage and situation is in equilibrium, it basically means that the electric field, the amount of band bending which

we have done earlier, is going to be one over q and the band bending of either E c E v or E i with respect to the Fermi level.

Fermi level remains constant and how much is the charge accumulated can also be calculated because we know from our earlier discussion that the number of holes can be given by the, number of holes in a intrinsic semiconductor and the difference between the E i, E i is this and E F s. So, the difference between the two will give E F minus E i over k T will give me the extra positive charge which is coming on the semiconductor side.

So, the amount of band bending can be calculated from these two equations, which we have considered earlier. And this this situation is known as the accumulation of charges. So, we have a capacitor now, whose capacitance is across this dielectric, it is just like the capacitance of a dielectric and in this particular condition, we have accumulation of charges in the semiconductor and that is why it is known as the accumulation stage.

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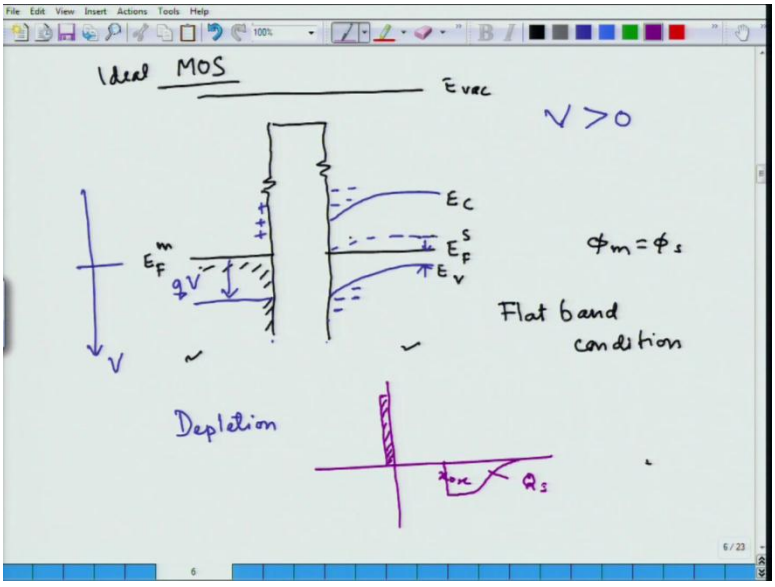

Similarly, I can take up a case, where where I will talk about when I am applying the voltage, which is going to be positive. So, if I am applying the positive voltage, if V is going to greater than 0. So, on that scale that we had drawn earlier now, we are increasing the voltage in positive direction and last time the Fermi level for the metal had moved up, this time it is going to be moving down, by q of V and in addition to moving

down, it is also going to with the similar equations that we have done earlier, it is going to band the electronic structure in the semiconductor downwards we can.

So, the new electronic structure is going to look like this and you can see immediately what is happening here is, the Fermi level is moving this is the difference between the Fermi level and the edge of the valence band it is moving away from the valence band, which basically means and the E i is also changing. If the Fermi level is moving away we are going to have a situation in which, the material is getting less, positive charge or negative charge, less positive means there are ionized acceptors here.

So, there is going to be negative charge accumulation in the semiconductor and equivalent to that, there will be a positive charge on the metal and this situation in which a p-type semiconductor is getting a opposite type of carrier is known as the depletion region, is depletion of the semiconductor and what is happening here is. Now, if I will measure the capacitance of this capacitor it is will be the capacitance, due to the dielectric and the capacitance due to the depletion region, which has been created in the semiconductor.

Now, what I want to do is I want to increase this V further to more positive, if I keep increasing this further as you can see what will happen is that, there I will be more band bending.

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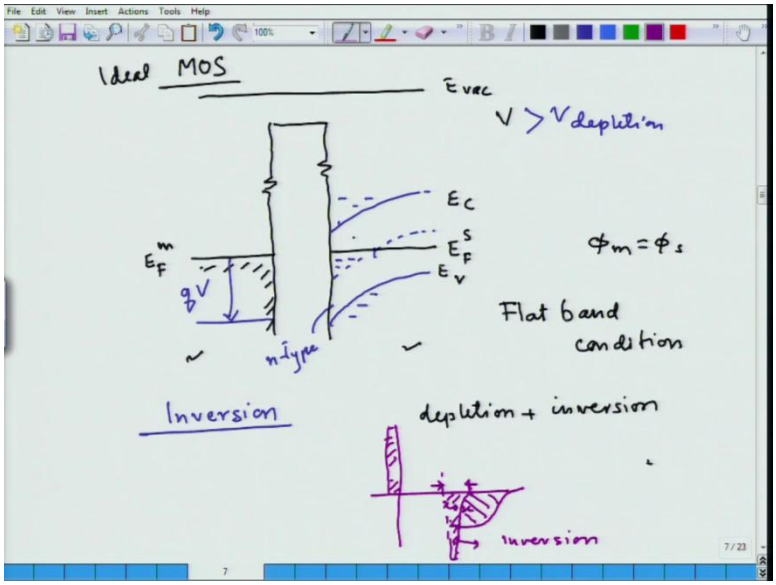

So, let us see what happens if there is going to be more band bending which means, V is now greater than the case of V depletion, where the depletion is started. So, if V is greater than the V depletion of the last side, then this means that I am going to now have a case, where this is going to be further down much more depressed on the Fermi level of the metal and I am going to have band bending, which is going to be quite extreme.

Now, this is a very interesting case because what is happening here is, a material which was p-type, Fermi level remains the same there is no current flowing in the semiconductor Fermi level, level remains the same, the material on this side is p-type because this is Fermi level is below the intrinsic level on the left side, it is Fermi level goes up. So, the material is actually becoming n-type.

And this particular region where you apply much higher positive voltage to a p-type MOS device is known as inversion, inversion because it is changing from a p-type to a n-type device and in this case, in addition to the negative acceptors, what we are having is the charge due to the the free charge which are going to be accumulated here, due to the inversion region. So, in addition to the depletion, in addition to the depletion we have the the inversion due to band bending.

Now, again the capacitance here is going to be capacitance of the dielectric, plus the capacitance of the depletion. So, if we look at all the three cases, what we have done is we have taken a ideal MOS capacitor, where the metal work function is same as the semiconductor work function, we applied a negative bias to it and we saw the accumulation of the charge carriers in the p-type semiconductor, then we applied a positive bias to it and we saw depletion of charge carriers in the semiconductor and if we continue to apply more positive bias it goes to a inversion region and that is what we have seen in terms of the band structure. The same thing, we can show in a charge distribution. So, if I look at same curves I would like to go back to my earlier slide.

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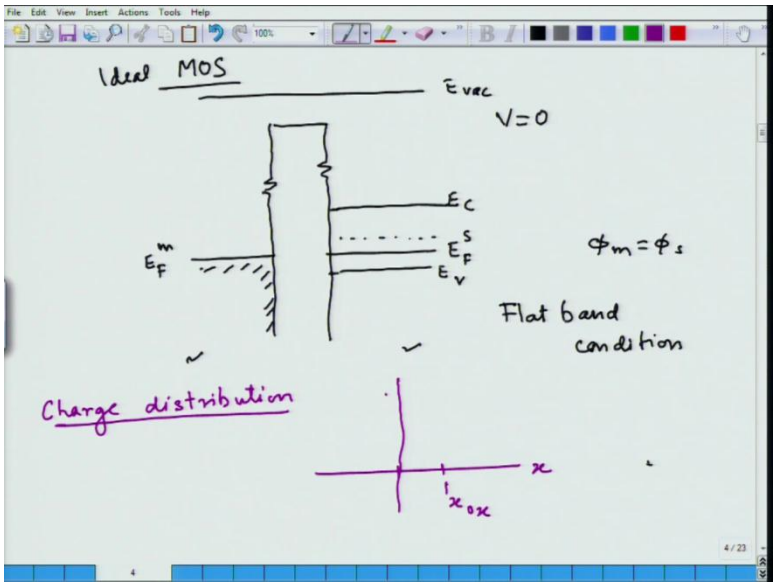

In this particular case, if I plot now for you what is the charge distribution inside this MOS ideal MOS capacitor. So, I am plotting now charge distribution. So, in the x axis, this is my oxide on this side, in this particular case I have no charge. So, I am plotting the x axis here, this is the oxide thickness x ox, but there is no charge either on the metal or the semiconductor.

So, there is no charge, when we have the ideal MOS capacitor, same thing if I now plot for the accumulation region, this is x ox this is the metal surface on the on the left side of of the metal we have negative charge. So, this is charge in the device. So, this is the total of this charge will be Q m the area will be Q m that I have plotted here and what is happening on the semiconductor side, we have the depletion region because of that we have a positive charge and I am going to show that positive charge more schematically, as if for the depletion region going like this.

So, this is the positive. So, if we look at now, the charge distribution in the depletion condition, charge distribution in the depletion condition is going to have positive charge on the metal side, this is a metal side x ox and negative on the semiconductor side, this is for the depletion Q of x. Now, let us look at what happens when we come close to the inversion condition, at that point we still have the positive charge on the metal side and in the semiconductor in addition to the depletion region because of the inversion we have free electrons in a charge, due to the inversion region.

We need to keep this in mind this inversion region is actually very, very small, very, very small in dimension, but in order to show it to you I am making it big, but this is a very thin charge distribution, almost delta like charge distribution at the edge of the oxide, in the in the semiconductor. So, now, if I look at the capacitance of this, it would be capacitance due to this oxide plus a capacitance due to the depletion layer. So, with all this charge distribution, if I plot what the capacitance looks like.

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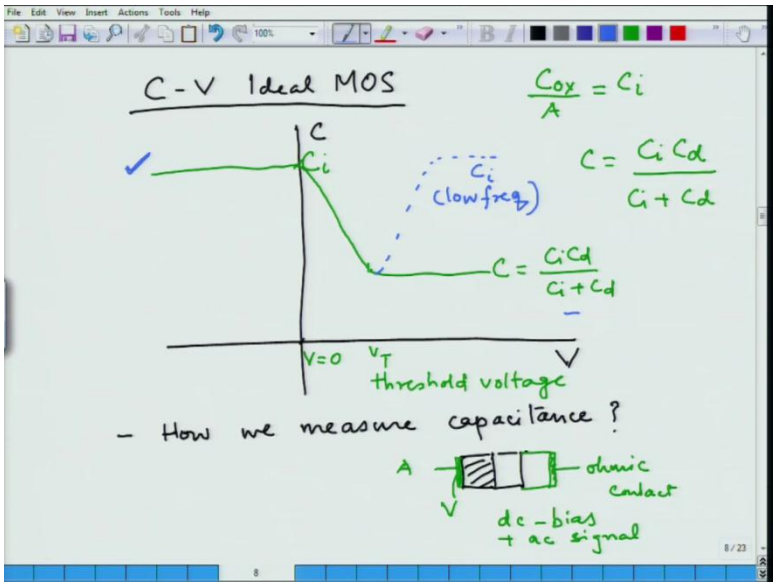

So, if I plot the capacitance versus voltage for the ideal MOS, for which we have already looked at the electronic structure and the charge distribution in the device and these are all equilibrium considerations, then I can plot the capacitance versus voltage and for this ideal MOS at 0, capacitance was there was no charge distribution, but was the capacitance 0, capacitance was not 0 and the reason for that is on how we measure capacitance.

So, in order to measure capacitance of this MOS structure, we normally apply. So, you have a metal, you have the oxide and then you will have the lets say semiconductor, on the semiconductor you will have ohmic contact on this side. So, that this does not become another device and you will have contact through the metal, from where you are applying the different values of voltages. Now, in order to measure the capacitance of this structure between these two metals, we normally apply a d c bias.

Now, when you are applying a d c bias for the measurement in addition to that, we apply a small a c signal. So, even when there is flat band condition and there is no charge in the device, when we apply this small a c signal I am going to measure a capacitance, which is going to be the fluctuations when the a c signal is applied and that fluctuation is going to give at V is equal to 0, which was the flat flat band condition.

I am to I am going to get capacitance of the oxide and normally rather than writing capacitance of oxide, we use capasisa capacitance of oxide divided by the area of the capacitor and area is this area because it will have another dimension to it. So, that will be the area of the contact and this we will call at, capacitance per unit area of the insulator.

So, we will have, in the flat band condition capacitance which is going to be that of the oxide only, when we go towards the negative voltage, which was the condition for accumulation as we we had seen that it is basically again capacitance across the oxides. So, this remains constant, when we go towards positive voltage the depletion starts and now the capacitance is going to be capacitance of the insulator times, the capacitance of that capacitance of the depletion area in the semiconductor and it will be given by this value.

So, as the depletion area grows I would see, the capacitance decreasing. Until a point where I start the inversion and that we call as threshold voltage, at threshold voltage we start the inversion and we will soon see what are the conditions or how we define threshold voltage, at this point up to the threshold voltage the depletion area in the semiconductor was increasing, but at this point the inversion layer starts and when we increase a voltage further, depletion layer does not change.

It is basically the inversion layer the charge accumulates in the inversion layer and if we if we, see that then basically the c remains constant beyond this threshold value which is given by the value C I C d C I plus C d. So, this is the the ideal C v MOS curve that we expect, but in reality it is a little bit dependent on the frequency and that is because if I do the measurement at a low enough frequency, then the depletion the the carriers are able to respond properly and the curve that I get at low frequency is after depletion inversion starts, I am going to get back the C i curve, this is what happens, if this capacitance measurement that I talked about is done at low frequency. So, the

capacitance measurement is dependent on the the a c signal that we apply during the measurement and at high frequency, it is going to be given going to be constant, since the carriers are not able to respond and move, you will get the capacitance which is going to be given by this term. So, this is the behaviour for capacitance for a ideal MOS. Now, as you can start seeing the use of this particular device, earlier when we had a dielectric capacitor, you had only one state.

Basically, if you apply a voltage you get a certain capacitance given by the material properties, but here we have a device because I can now change, the capacitance of this device depending on what voltage I apply, I can have a condition I can have a state of the device, where it is at this capacitance and I can have a second state of the device, it if at higher positive voltage, where the capacitance is different and you can start seeing it is use as a memory element already. So, depending on what voltage is applied to the device, it will be work it will work as a memory element.

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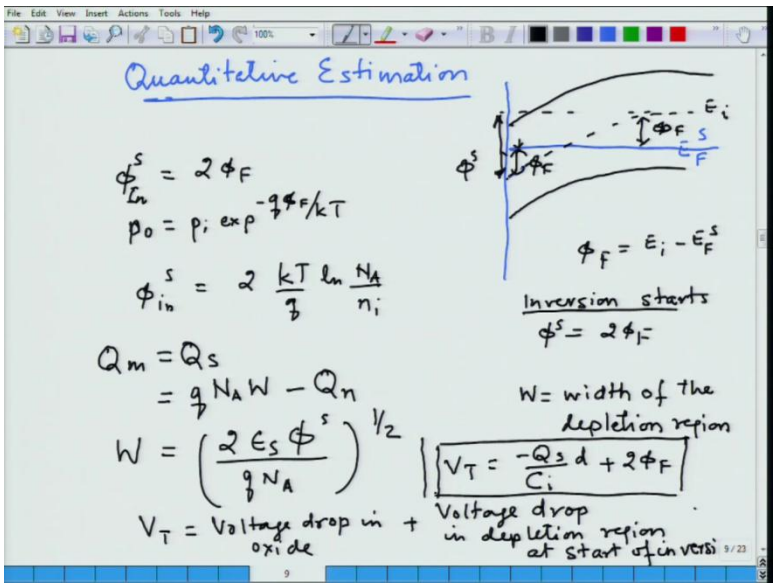

So, having done this qualitative expression for what the C v of ideal MOS looks like, let us do quantitave quantitative estimation of the threshold voltage, which is going to be a important parameter when we talk about the transistor and in order to do the quantitative estimation of the threshold voltage for ideal MOS, we enlarge the situation in which we have inversion. So, we are going I am going to define some terms in order to, do the maths that is related to inversion.

So, my Fermi level is in the semiconductor remains constant, there is no current flowing and in the inversion situation the E i has band enough. So, that it is giving rise to the inversion. So, if this is E i and this is the phi of the Fermi level. So, phi of F is being defined for a p-type semiconductor here, as the difference between the intrinsic level minus the semiconductor Fermi level.

And I am going to now quite arbitrary decision that I am going to say inversion starts I am going to say inversion starts, when the potential difference at the surface phi s which is given by this term here, phi s and we have used phi for the work function of semiconductor. So, let me make it phi s, at the surface is equal to 2 of phi F which basically means, the now it is as n-type as it was p-type.

So, at this surface now, phi s is equal to and phi s is defined as one second, how much has it bent, how much is the intrinsic level bent. So, phi s when it is equal to 2 of phi F which means this is also phi f, then we say this is the start of the inversion. Now, with this condition I can calculate, what would be my threshold voltage at which the band bending is enough to create, the change in the intrinsic Fermi level at the at the interface equivalent to 2 of phi of F.

So, what is this phi of s, phi of s is equal to which is at the inversion condition, we are calculating the threshold voltage when the inversion starts, is going to be equal to 2 of phi of f. And I know how to calculate phi of f, because I know the condition where n 0 in this case p 0, for the p-type semiconductor will be given by exponential minus q of phi of times k T over q l n acceptor concentrations divided by n i.

So, I know how much band bending is there, at the inversion condition I also know that from the charge discussion that the total charge on the metal is equal to the total charge in the semiconductor, what is the total charge in the semiconductor, is the charge due to the depletion region and once again I am going to invoke the approximation that we did in the diode, we assume that the acceptor doping is uniform throughout the semiconductor.

So, the total charge in that approximation is going to be q times the acceptor concentration, multiplied by the width of the depletion region. So, w is the width of that width of the depletion region. So, this is the total charge in the depletion due to depletion

region minus the charge which is there due to the inversion of the, inversion caused by the band banding.

Now, I can do this calculations, similarly that I have done earlier for p-n junction and calculate what is what is the w, w can be estimated and without deriving I will use the expression that we have used for p-n junction, where I will use a highly doped p-type. And highly doped n-type and depletion only in the p-type layer. In that case, the width will be given by dielectric constant of the semiconductor times phi of s divided by q times N A to the power half.

So, now, I know the width. So, I can calculate what is my charge, what is the charge due to in the depletion region, now phi of s at the inversion condition is given to me. So, with with those conditions I can calculate, what would my threshold voltage. So, the threshold voltage is going to be equal to, the voltage drop in the oxide, voltage drop in oxide plus the voltage drop in depletion region at inversion point at start of inversion and I have defined the condition for inversion is condition for inversion is given by 2 times phi f.

So, this number is going to be then given by, voltage drop in oxide is a simple factor which is given by the charge, in the metal or the semiconductor divided by the capacitance per unit area multiplied by the thickness of the oxide plus the voltage drop is in the semiconductor is nothing but 2 times phi of F. So, this is my threshold voltage at the inversion point. So, this gives me an estimate of finding out at what point in the MOS capacitor I get inversion condition. Now, this is important when we come to discussion of transistor because at this inversion condition, as we discussed earlier, we basically have a very high charge density at the interface it is almost like a channel of charges which can then be used and manipulated to make the transistor.

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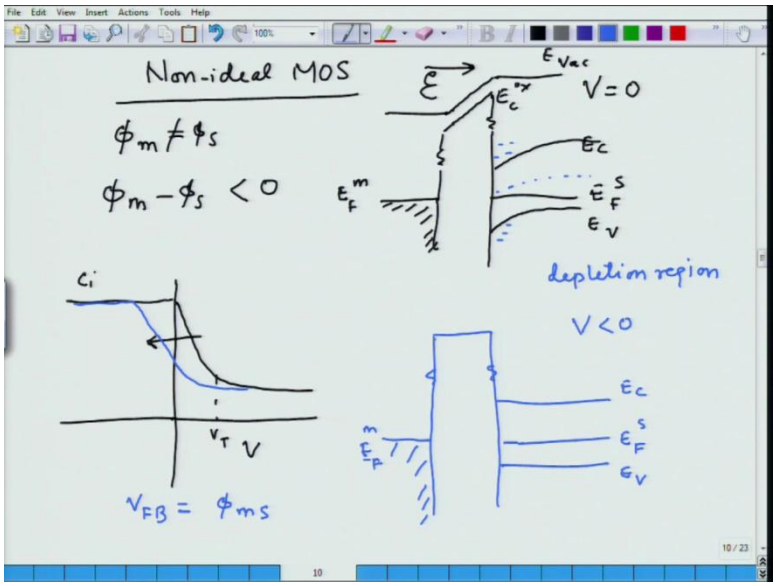

So, we will use this data later. Now, this condition all the discussions, so far was for a ideal MOS, if the MOS is not ideal, if you have a non-ideal MOS. So, what are the non-ideal factors that can come into picture, the first one is which is we very conveniently assume that phi m is equal to phi s the work functions were equal, but they may not be equal. So, let us look at example when they will not be equal, if they are not going to be equal, let me make an exemption let that the situation is such that phi m minus phi s is less than 0. So, if we go back to our earlier definition which means phi m is smaller compared to the phi s value, if this is there then my in this condition if I draw the energy band diagram at V is equal to 0, earlier I had applied band condition I am not going to have flat band condition anymore because I need to equate the Fermi level on both sides.

So, if I equate the Fermi level of the metal, across the oxide this is going to be the Fermi level of the semiconductor, Fermi level of the metal and we have the vacuum level, which is phi m is less is a smaller and then we have the vacuum level for the semiconductor if phi s is large, which basically means that the difference of this is to be taken up by the oxide and here, this means that there is going to be a field due to this non-ideality.

Earlier, there was a flat oxide a conduction band and because of this non-ideality, this is the vacuum level and the conduction band is here and the valence band is here E c and E v and I have the oxide is having this is the E c of the oxide, then that is going to be a

field across it. Now, if there is going to be a field across it, which means as going to be charge accumulation, which means this is not going to be flat anymore and what is going to be the charge, if E F was the smaller than E s which means the negative charge is going to come on this side and there is going to be band bending downwards.

So, in equilibrium for a non-ideal MOS there is going to be downwards band bending, E i is here and as a result there is going to be accumulation of negative charge. So, even when you apply no voltage, there is a depletion region, there is a depletion region in a non-ideal phi m s and in this particular non-ideal MOS in order to get the flat band, we will have to apply a voltage which is going to be negative. If I apply a negative voltage and I use a same consideration that I have used earlier, which means I am going to change the Fermi level of the metal at that point I will get the flat band condition.

So, the flat band condition will come which is E F s when a negative bias is applied sorry it is a flat band condition which means, it is remain same. So, if you compare the non-ideal MOS with the ideal MOS, the c v characteristic of non-ideal MOS with the ideal MOS, the ideal MOS c v characteristics had c i up to 0 voltage and then a depletion and inversion on set of the inversion at v T.

And you can immediately see, if we have the situation where it is non-ideal even at v is equal to 0, that is going to be already a depletion, which means this curve is going to be shifted, in this direction and for a non-ideal thing schematically it is going to be something like that, which means a non-ideal if phi m s is not 0 and it is less than 0 there is going to be a shift towards left for the c v curves.

So, this is the non-ideality that one has to built in and in this case the flat band voltage is going to be equal to at which you will get flat band, is going to be equal to phi of m s I have to apply the difference of the phi of m s in order to get the flat band condition, and that would shift the ideal c v curve towards a right and left depending on what the conditions.

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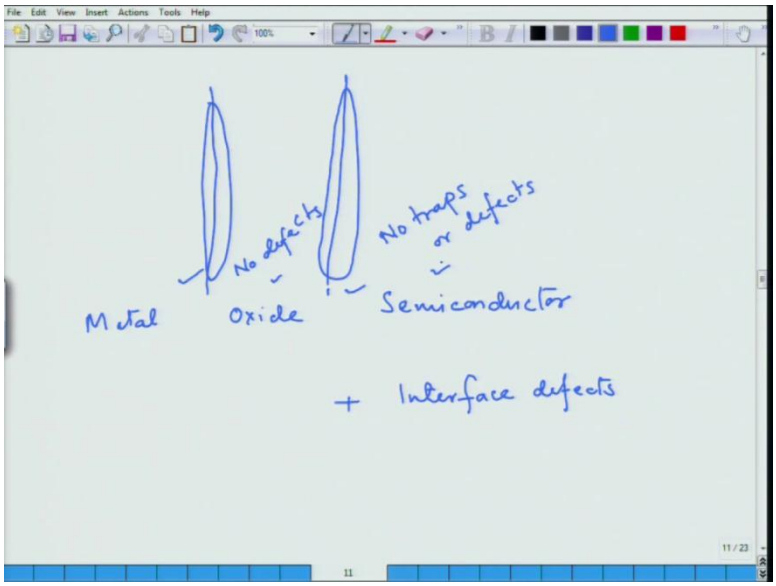

There are more non-idealities that are occurring in the MOS device and just to point out there are few and I am going to make this a bigger picture here because when we made all these charge accumulation and depletion, in metal oxide and semiconductor I am only looking at the accumulation in the material but I assume there are no defects of course, metal we do not worry about defects, that there are no defects here, which in advance courses you will see that oxide is full of charge defects.

And hence, there are not going to be only charges at the interfaces I will be charges in the oxide and even here, I assumed no traps of defects and in module 3, we have already seen that there are traps and defects in in a semiconductor, which define the generation recombination mechanisms. So, there will be changes in the ideal MOS behaviour because of these traps and defects, in addition to these things which are in the material, we have what is known as the interface defects. And they also play a part in semiconductor devices and these interface defects are basically at these points and they can change the c v curve, because they can they can trap charges or they can release charges, depending on their behaviour and then that will change your c v curve completely.

Now, this may be a bad news for a ideal MOS, but it is also a good news for material characterization because if you want to characterize your material, this turns out to be the c v of the MOS device, it turns out to be a very good device in different modes you can

study whether whether you can study the interface defects or the material oxide defects or the semiconductor defects or necessarily semiconductor defects, but the oxide defects have been studied using this MOS c v curves. Now, finally I would like to once, now that you know that you have a device who capacitance you can control by changing the voltage, you can use it in many ways and some applications which are, which come to mind at this point and which are very popular also.

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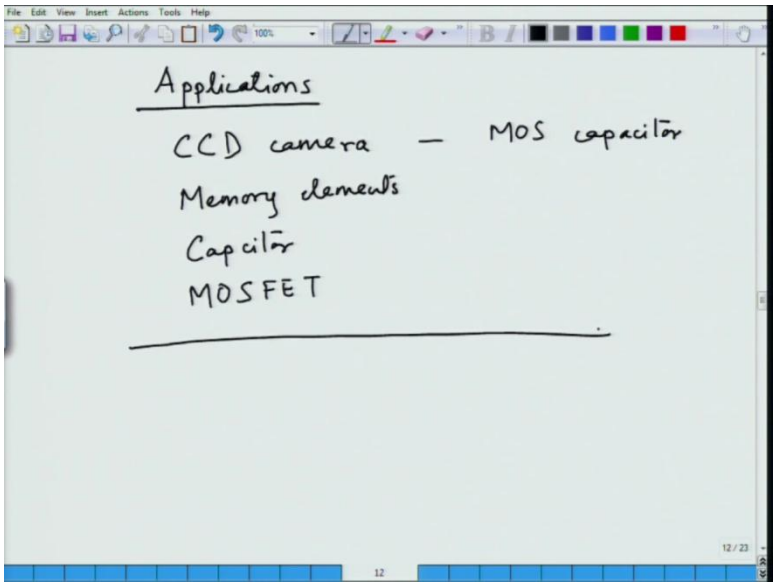

So, everybody has heard of CCD camera and the device that stores the charge or the information there is a MOS capacitor. So, a then there is another application as I already mentioned it can be used as a memory element, because now you have two states of capacitance depending on what voltage you apply, it can be used as a capacitor itself in a integrated circuit and of course, it is a very important part of a MOSFET, the MOS device, which is which basically is dominating most of the electronic circuit fabrication, the MOSFET is a very important device.

So, with this I would like to conclude our discussion on MOS capacitor, we have done qualitatively what is the c v curve of from MOS capacitor, what is a threshold voltage and what are the some of the non-idealities which will change the curve, and these can be then used for characterising the material itself. And some of the important applications of the capacitors themselves and their applications in other integrated circuits.