B.Sc. DEGREE EXAMINATION, APRIL 2018.

III YEAR VI SEMESTER

Core Elective - Paper III - MICROPROCESSOR INTERFACING & APPLICATIONS

Time : 3 Hours Max. Marks : 75

SECTION A – (10 × 2 = 20 marks)

(Q. No. 1-12)Answer any *TEN* questions

1. Define machine cycle and T state.
2. Where are delay programs used?
3. Write a delay subroutine to generate a time delay of 1msec using single register.
4. Define memory mapping in memory interfacing.
5. What is the necessity of the wait state generator?
6. Draw the logic circuit to generate control signal in 8085.
7. How many address lines are required to address

a) 2KB b) 64KB c) 1MB and d) 1GB of memory locations.

1. What are the types of I/O interfacing.
2. Distinguish between Hardware and Software interrupts in 8085.
3. Explain the need and use of EI and DI instructions in 8085 interrupts.
4. What is programmable peripheral device?
5. What is Handshake Port?

SECTION B – (5 × 5 = 25 marks)

(Q. No. 13-19)Answer any *FIVE* questions

1. Tabulate the machine cycles in 8085 along with their status & control signals in respective operations like.
2. Opcode Fetch
3. Memory Read
4. Memory Write
5. I/O Read
6. I/O Write
7. Explain how the AD0 - AD7 bus of 8085 CPU is demultiplexed using latch 74LS373
8. Distinguish between I/O mapped I/O and memory mapped I/O for Input / Output interfacing with 8085 CPU
9. Explain
	1. SIM instruction Format.
	2. RIM instruction Format.
10. Explain with circuit how 8255 can be interfaced to 8085. Choose convenient address.
11. Draw the circuit to display numbers from 0to 9 and tabulate the BCD codes for respective seven segment display of numbers.
12. Give the basic concept of memory interfacing.

[P.T.O.]

SECTION C – (3 × 10 = 30 marks)

(Q. No. 20-24)Answer any *THREE* questions

1. Sketch and explain the timing diagram for the instruction MVI A, 40H of 8085.
2. Design the memory interfacing for a 8085 system with memory of ROM : 2K x 8 bit

 the starting address for ROM & RAM is 0000H and 1000H respectively. Indicate clearly and explain the decoder and different control circuits used.

1. Draw the timing diagram for the OUT instructions of 8085 CPU and explain in detail. Assume the Output port address.
2. List and explain the 8085 instructions related to interrupts.
3. a. Discuss the organisation and architecture of 8255 programmable peripheral interface

 IC with a functional block diagram

b. Illustrate the different modes of operations of 8255.