SHRIMATHI DEVKUNVAR NANALAL BHATT VAISHNAV COLLEGE FOR WOMEN
(AUTONOMOUS)
(Affiliated to the University of Madras and Re-accredited with 'A+' Grade by NAAC)
Chromepet, Chennai — 600 044.
B.Sc. END SEMESTER EXAMINATIONS NOVEMBER-2022
SEMESTER - I
21UCSCT1002 - Digital Computer Fundamentals and Architecture

Total Duration : 2 Hrs 30 Mins. Total Marks : 60

Section A

Answer any **SIX** questions $(6 \times 5 = 30$ Marks)

1. Convert the following decimal numbers into the specified number format
   i) 550.50 to octal
   ii) 1938.24 to hexadecimal.
   iii) 175.87 to binary
2. Distinguish the working of OR gate and XOR gate with neat circuit diagram and truth table.
3. State and prove the De-Morgan's Theorem using truth table.
4. Demonstrate how does JK flip flop work with a neat circuit diagram and truth table.
5. Summarize the hardware implementation of logic micro-operations and explain any 6 logic micro-operations with truth table for 2 variables.
6. Is implied and immediate address modes have no address field? Prove with your answer.
7. Classify Relative, Indexed and Base Register Addressing mode.
8. Dissect how the Direct Memory Access(DMA) works and prove whether the transferring speed is fast in DMA when compare to asynchronous data transfer.

Section B

Answer any **THREE** questions $(3 \times 10 = 30$ Marks)

9. Convert the following decimal numbers to hexadecimal number.
   i) 1231.275 ii) 673.18 iii) 1998.425
10. Simplify the Boolean function F with four variables together with Don't care condition D in sum of product method.
    F(A,B,C,D)= Σ(0,1,2,3,7,8,10)
    D(A,B,C,D)= Σ(5,6,11,15)

Contd...

11. Differentiate zero, one, two and three address instructions with necessary example.
12. Sketch the flow chart of the hardware implementation of Addition and Subtraction of signed magnitude numbers.
13. Is cache memory a high speed memory? Justify your answer and explain the working principle of cache memory.

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