SHRIMATHI DEVKUNVAR NANALAL BHATT VAISHNAV COLLEGE FOR WOMEN
(AUTONOMOUS)
(Affiliated to the University of Madras and Re-accredited with 'A+' Grade by NAAC)
Chromepet, Chennai — 600 044.
M.Sc. - END SEMESTER EXAMINATIONS NOVEMBER - 2022
SEMESTER - I
14PCSCE1001 - Computer Architecture

Total Duration : 2 Hrs 30 Mins. Total Marks : 60

Section A

Answer any **SIX** questions $(6 \times 5 = 30$ Marks)

1. Describe about complements.
2. Describe Array Multiplier.
3. Compare Isolated and Memory mapped I/O.
4. Illustrate the need for virtual memory.
5. What is instruction format? Explain two address instruction with example.
6. Draw the block diagram of BCD adder.
7. Describe handshaking in data transfer.
8. Ascertain how best the working of Cache memory is better.

Section B

Part A

Answer any **TWO** questions $(2 \times 10 = 20$ Marks)

9. Illustrate in detail about Logic Micro operations.
10. Apply pipeline processing to implement four segment CPU pipeline.
11. Justify Booth's multiplication is suitable for multiplication of signed 2's complement numbers.
12. Asses the importance of DMA controller.

Part B

Compulsory question $(1 \times 10 = 10$ Marks)

13. Recommend the suitable application area of associative memory with example.

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